Multi-mode Imager with Pinned Photo Region Photoreceptors

INVENTOR

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BACKGROUND OF THE INVENTION

1.   Field of the Invention.

This invention relates to electronic imaging devices, and in particular to a CMOS imager incorporating a photoreceptor array and a multi-mode controller.

2.   Related Art.

Electronic imaging devices ("imagers") find use in a broad range of applications in many distinct fields of technology including the consumer, industrial, medical, defense and scientific fields. Imagers use an array of photoreceptors to convert photons bearing image information into electrical signals representative of the image.

In recent years, CMOS imagers have become a practical implementation option and provide cost and power advantages over other technologies (such as charge coupled devices). A conventional CMOS imager is typically structured as an array of imager cells, each of which includes a photoreceptor approximately reset to a known potential in preparation for integration and readout of an image. The performance of a CMOS imager depends heavily on the performance of the individual imager cells.

In the past, the imager cells took the form of either passive photoreceptor cells, active photoreceptor cells, or transfer gate active photoreceptor cells. The passive photoreceptor cells typically included a photodiode for collecting photocharge and a single access transistor to connect the photodiode to a readout bus. However, passive

photoreceptor cells, while having high quantum efficiency, were plagued by large amounts of noise.

As a result, imagers began to incorporate active photoreceptor cells. The active photoreceptor cells included a photoreceptor, and either three or four support transistors. The support transistors included a reset transistor, source follower transistor (for buffering and amplifying the collector photocharge), and an access transistor for connecting the photoreceptor to a readout bus. In transfer gate active photoreceptor cells, a fourth transfer gate transistor was used to transfer photocharge from the photoreceptor to a sense node, thereby allowing correlated double sampling, and a corresponding decrease in noise.

During integration, a photoreceptor cell sets up a potential well that collects electrons generated by incident photons. The potential well, however, has a limited charge capacity. As a result, it was possible for bright light to generate enough electrons to substantially fill the potential well of the photoreceptors in an imager, thereby yielding a washed out image. Thus, prior photoreceptor cells were not tailored to provide adequate response over a wide range of light levels.

Furthermore, prior imagers implemented a progressive readout technique that sequentially transferred charge from a row of photoreceptors to their respective sense nodes, then through respective amplifiers to a column bus. However, while one photoreceptor row was being readout, the image information stored in the remaining photoreceptor row was susceptible to noise from the photoreceptor structure itself, as well as from additional incident photons. Thus, the image acquired by the photoreceptor array changed as the image was being readout.

A need exists for an improved imager cell that addresses the problems noted above and other previously experienced.

SUMMARY

An improved imager is arrived at by incorporating a mulit-mode controller in an imager. The imager may be broadly conceptualized as an light detector with low noise characteristics that is configurable for a wide range of charge capacity, for a wide range of light levels, as compared to conventional imager cell implementations.

The imager may be implemented as an array of imager cells coupled to a multi-mode controller. The multi-mode controller includes circuitry that implements several modes of operation, including a high-light mode, a low-light mode, and a Snap mode. As explained in more detail below, the high-light mode provides charge accumulation in a photoreceptor potential well, a readout potential well, and a sense node potential well. The low-light mode provides charge accumulation in the photoreceptor potential well and constrained by an integration potential well. The Snap mode of operation simultaneously transfers accumulated charge for a set of the imager cells to their sense nodes.

During the high-light mode, the multi-mode controller applies a V+ integration voltage during an integration period to a photoreceptor readout gate, thereby allowing charge to accumulate in the readout potential well. In addition, the multi-mode controller may select one of a plurality of V+ integration voltages for setting up a selected charge capacity in one of the imager cells. Thus, the V+ integration voltage may be increased to provide charge capacity to address increased light levels.

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The imager cells may be implemented using a pinned photoreceptor, a transfer gate, a reset transistor, an access transistor, and an output amplifier. The photoreceptor may be, for example, a photodiode. Furthermore, the imager cells may include anti-reflective coatings to improve performance.

Other implementations, methods, features and advantages of the invention will be or will become apparent to one with skill in the art upon examination of the following figures and detailed description. It is intended that all such additional systems, methods, features and advantages be included within this description, be within the scope of the invention, and be protected by the accompanying claims.

BRIEF DESCRIPTION OF THE FIGURES

The components in the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principals of the invention. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

Figure 1 shows an imager cell with control circuitry.

Figure 2 shows an imager cell with a pinned photo region.

Figure 3 illustrates an imager including a multi-mode controller and an array of photoreceptors.

Figure 4 depicts a method of controlling an imager.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 presents a high level view of an imager cell 100. The imager cell 100 (descried in more detail below) includes a photoreceptor 102, a transfer gate 104, and a

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sense node 106. A reset transistor 108 is provided to reset the sense node 106. The source follower amplifier 110 buffers and amplifies the sense node 106 during readout to the column bus through the select transistor 112.

Turning next to Figure 2, that figure presents a more detailed view of an imager cell 200. The imager cell 200 is formed in a p-type substrate 202 and includes a photoreceptor 204, transfer gate 206 and sense node 208. A reset transistor 210 provides a mechanism for approximately resetting the sense node 208 to an initial level, while the source follower output amplifier 212 provides sense node 208 output buffering and amplification. A potential well diagram 214 illustrates the variation in electric potential across the imager cell 200.

As shown in Figure 2, the transfer gate 206 includes a photoreceptor readout gate 216, supporting gate oxide 218, and the p-type substrate 202. The photoreceptor 204 is formed as a photodiode including a pinned photo region 220 and an n- cathode region 222. The pinned photo region 220 is "pinned" because it is tied (or "pinned") to the potential of the substrate 202, typically ground or zero volts. Pinning the transfer generally suppresses dark current, which leads to an improved signal to noise ratio because fewer dark current electrons (i.e., noise electrons) contribute to the output signal. In addition, the photoreceptor 204 optionally includes an antireflective coating 224. The anti-reflective coating 224 may be formed, for example, from a 100 Angstrom layer of oxide and a 250 Angstrom layer of Silicon Nitride. The sense node 208 is formed from an n+ contact region 226 and p-type substrate 202.

In general, the p-doping may be accomplished using _____, while the n-doping may be accomplished using _____, and the p++ doped pinned region 220 may be

formed by _____. Note that the transfer gate 206 is disposed between the photoreceptor 204 and the sense node 208 in order to transfer charge between the photoreceptor 204 and the sense node 208. Note also that the transfer gate 206 includes a transistor gate structure (i.e., the photoreceptor readout gate 216). As explained in more detail below, the imager cell 200 sets up a potential well profile that allows charge to transfer through the transfer gate 206 depending on photoreceptor control clocks.

The operation of the imager cell 200 in low-light mode is now discussed with reference to the potential well diagram 214 and the photoreceptor control clock 228. Note that the photoreceptor control clock 228 varies between a V- level during an integration period 230 and a V+ level during a readout period 232. The duration of the integration period 230 and the readout period 232 vary in accordance with the desired operating speed of the imager cell 200. In one implementation, for example, the duration of the integration period 230 is approximately _____, while the duration of the readout period 232 is approximately _____.

Note first that the photoreceptor 204 establishes the photoreceptor potential well 234 in the substrate 202 and that the sense node 208 establishes a sense node potential well 236 for ultimately holding the charge accumulated in the charge collection well 234. During the integration period 230, the integration voltage V- establishes the integration potential well 238 in the substrate 202. At this time, photons incident on the photoreceptor 202 produce electrons that are captured in the integration potential well 234 and constrained by the photoreceptor potential well 238.

During readout after the integration period 230, the readout voltage V+ establishes the readout potential well 240 in the substrate 202. At this time, electrons captured in the photoreceptor potential well 234 propagate through the transfer gate 206 to the sense node potential well 236. Under control of an imager cell readout clock (which turns on the select transistor 112), the source follower amplifier 212 then buffers and amplifies the sense node potential onto the column bus. After readout, the reset gate 210 activates under control of a sense node reset clock to approximately reset the sense node 208 to a known potential.

Turning next to Figure 3, that figure shows an imager 300 including a multi-mode controller 302 ("the controller 302") coupled to a photoreceptor array 304. The photoreceptor array 304 may be formed from imager cells 200 arranged in a predetermined pattern (which need not be square or rectangular). The controller 302 provides the photoreceptor control clocks 306, the sense node reset clocks 308, and the imager cell readout clocks 310. The controller 302 also provides several modes of operation, including a high mode, a low mode, and a Snap mode. Conventional digital circuitry may be used to implement the controller 302 according to the high-light, low-light, and Snap operational mode descriptions discussed below.

In particular, the controller 302 may by constructed as _____. **JIM - INSERT MORE DETAIL ON HOW THE CONTROLLER IS IMPLEMENTED - IS IT A PROCESSOR CORE, OR ALL CUSTOM LOGIC?**

Typically, the controller 302 operates the imager 300 in the low-light mode. In the low-light mode, the controller 302 asserts the photoreceptor control clock 228 as noted above. In particular, the controller 302 asserts a photoreceptor control clock with

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an integration period 224 and a readout period 222. Thus, the photoreceptor potential well 234 provides the charge capacity to accumulate electrons produced by incident photons. The charge capacity is generally sufficient for imaging in low-light levels. In other words, the controller 302 selects the low-light mode when the controller 302 determines (or is explicitly commanded by an operator through input keys) that the measured, predicted, or modeled quantum efficiency and charge capacity of the charge collection well 234 will not be overwhelmed by electrons generated based on current lighting conditions.

After the integration period 230, the photoreceptor control clock 228 switches to a V+ readout voltage during the readout period 232. As a result, the readout potential well 240 is set up and electrons captured in the photoreceptor potential well 234 propagate through the transfer gate 206 to the sense node 208. Subsequently, the controller 302 asserts the imager cell readout clock 310 to couple the sense node 208 through the source follower amplifier 212 and the select transistor 112 onto the column bus. External circuitry then produces a digital sample charge level in the sense node 208. After the external circuitry is finished reading the sense node 208, the controller 302 asserts the sense node reset clock 308 to approximately reset the sense node 208 to a known potential in preparation for the next readout cycle.

In certain instances, the controller 302 operates the imager 300 in the high-light mode. In the high-light mode, the controller 302 asserts the V+ voltage as the integration voltage during an integration period (rather than the V- voltage). As a result, the potential well existing in the substrate 202 during integration includes the photoreceptor potential well 234 (under the photoreceptor 204), the readout potential

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well 240 (under the transfer gate 206), and the sense node potential well 236 (under the sense node 208). In other words, in high-light mode, the readout potential well 240 and sense node potential well 236 are also used to accumulate charge generated by incident photons.

Note that in the low-light mode described above, the charge collection well existing in the substrate 202 during integration essentially corresponded to the photoreceptor potential well 234. In other words, during the low-light mode, the photoreceptor potential well 234 is constrained by the integration potential well 238 set up by the V- integration voltage.

Thus, in the high-light mode, a greater charge capacity exists in the substrate 202. As a result, when the controller 302 selects the high-light mode based on the measured, predicted, or modeled quantum efficiency and charge capacity of the charge photoreceptor potential well 234 (or when the controller 302 is explicitly commanded by an operator through input keys), the imager cell 200 provides a charge capacity that can capture an amount of electrons that might otherwise overwhelm the low-light photoreceptor potential well 234 as constrained by the integration potential well 238.

In high-light mode, the controller 302 performs readout in the same manner as noted above with respect to the low-light mode. In particular, after the integration period, the controller 302 asserts the imager cell readout clock 310 to couple the sense node 208 through the source follower amplifier 212 and the select transistor 112 onto the column bus. External circuitry then produces a digital sample charge level in the sense node 208. After the external circuitry is finished reading the sense node 208, the

controller 302 asserts the sense node reset clock 308 to approximately reset the sense node 208 to a known potential.

Note that during high-light mode as the integration voltage V+ increases, so does the depth of the potential well 240, and thus so does the overall charge capacity level for the photoreceptor 202. As a result, during conditions of bright light, for example, the controller 302 may increase the integration voltage V+ to enhance the charge collection capacity level in the photoreceptor 202 (and thereby reduce blooming or washout, as examples). To that end, the controller 302 may be preprogrammed with a selection of V+ integration voltages to apply, during high-light mode, to the photoreceptor readout gate 216, as selected by external input, or in coordination with measurements received from external light sensors or the like.

As noted above, the imager cell 200 may also operate in what is referred to as a "Snap" mode in conjunction with the low-light mode. In the Snap mode, the controller 302 asserts the V+ readout voltage 232 of the photoreceptor control clocks 306 for multiple imager cells 200 simultaneously. The result is that the charge collected in a set of photoreceptors 200 is simultaneously transferred into the sense nodes 208 of each respective photoreceptor 204. The Snap mode thus provides a snapshot at an instant in time of the charge collected in the set of photoreceptors 200 to obtain image information undisturbed by noise arising during, for example, a sequential readout process.

As an example, numerous imager cells 200 may be organized into an array to form a CMOS imager. The controller 302 may then select two or more imager cells 200 as a set of photoreceptors 200 for the next Snap operation. As examples, the set

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may include all the photoreceptors 200 that form a rectangular sub-array in the center of the CMOS imager, a stripe of predetermined width vertically through the center of the CMOS imager, or every other imager cell 200 in the CMOS imager.

Turning next to Figure 4, that figure illustrates a flow diagram of a method for controlling an imager. Initially, the controller 302 determines (302) an operating mode. For example, the controller may select either a high-light or a low-light operating mode based on external light sensors, operator input, and the like. In high-light mode, the controller 302 selects (404) a V+ integration voltage to setup a desired charge capacity level in the substrate 202. As noted above, the integration voltage V+ may be increased to increase the charge capacity, for example, by selecting between one or more preset integration voltage options in the controller 302. After the controller 302 selects the V+ integration voltage, the controller 302 asserts (406) the V+ integration voltage during an integration period to accumulate electrons generated by incident photons.

On the other hand, in the low-light mode, the controller 302 asserts (408) a V- integration voltage during an integration period. Electrons generated by incident photons are then collected in the photoreceptor potential well 234. In optional conjunction with Snap mode operation, the controller 302 then asserts (410) a V+ readout voltage to a set of photoreceptors 200. Captured charge is thereby simultaneously transferred to the sense nodes 208 associated with each photoreceptor 204 that is part of the Snap operation. It is noted that it is not necessary to use the Snap mode, however. In other words, conventional photoreceptor array readout techniques are also suitable.

The controller 302, in both high-light mode and low-light mode then proceeds to assert (412) imager cell readout clocks to the access transistors 112. As a result, the sense nodes 208 are amplified and buffered by the source follower amplifiers 212 through the access transistors 112 onto the column bus. After readout, the controller 302 then asserts (414) the sense node reset clocks to return the sense nodes 208 approximately to a known potential.

In this manner, the imager provides enhanced performance light sensors using a multi-mode controller. The Snap mode provides a snapshot at an instant in time of the charge collected in a set of photoreceptors to obtain image information undisturbed by noise. The high and low modes provide a selective charge capacity to accommodate wide variations in light level. The selectivity in integration voltage in high-light mode also provides a configuration charge capacity for the photoreceptors.

While various embodiments of the application have been described, it will be apparent to those of ordinary skill in the art that many more embodiments and implementations (e.g., using a different form or representation of quantization of the photoreceptor noise range) are possible that are within the scope of this invention. Accordingly, the invention is not to be restricted except in light of the attached claims and their equivalents.